What is claimed is:

1. A semiconductor integrated circuit comprising:

a function block arranged on a substrate;

a first buffering cell arranged adjacent to a first side of the function block;

a second buffering cell arranged adjacent to a second side adjacent to the first side of the function block; and

signal wiring passing over the function block obliquely relative to the first side and the second side, connecting the first buffering cell and the second buffering cell.

2. The semiconductor integrated circuit of claim 1, further comprising:

a first signal wiring extending in an X direction, which extends obliquely relative to the signal wiring; and

a second signal wiring extending in a Y direction, which is perpendicular to the first signal wiring and extends obliquely relative to the signal wiring.

3. The semiconductor integrated circuit of claim 2, wherein the signal wiring is arranged in a layer higher than the layer in which the first signal wiring and the second signal wiring are arranged.

4. The semiconductor integrated circuit of claim 2, wherein the signal wiring has an intersecting angle either 45 degrees and 135 degree relative to either of the first signal wiring and the second signal wiring.

5. The semiconductor integrated circuit of claim 1, wherein the signal wiring is a global signal wiring including one of a data bus and an address bus, arranged substantially in the entire area on the substrate.

6. The semiconductor integrated circuit of claim 1, wherein the first buffering cell and the second buffering cell are arranged outside of the function block.

7. The semiconductor integrated circuit of claim 1, further comprising a wave guide arranged adjacent to the signal wiring and extending substantially parallel to the signal.

8. A semiconductor integrated circuit comprising:

a function block arranged on a substrate;

a plurality of signal wirings having a length shorter than a length of a side of the function block on the substrate;

a plurality of buffering cells electrically connected in series between each of the signal wirings; and

a signal wiring passing obliquely across the corner between a first side and a second side of the function block, which connects the buffering cells arranged adjacent to the first side and adjacent to the second side adjacent to the first side of the function block.

9. A semiconductor integrated circuit comprising:

a function block arranged on a substrate;

a plurality of buffering cells arranged regularly in the function block at an appointed interval; and

a signal wiring extending obliquely relative to a side of the function block, which is connected between adjacent buffering cells.

10. The semiconductor integrated circuit of claim 9, wherein each of the buffering cells comprises a first buffering cell and a second buffering cell having different drive abilities respectively.

11. The semiconductor integrated circuit of claim 9, wherein the signal wiring is a global signal wiring including one of a data bus and an address bus, arranged substantially in the entire area on the substrate and passes over the function block.

12. A method for manufacturing a semiconductor integrated circuit comprising:

arranging a function block on a substrate;

arranging a signal wiring which passes over the function block obliquely relative to a first side and a second side adjacent to the first side of the function block; and

arranging a first buffering cell connected to one end of the signal wiring, adjacent to the first side of the function block and a second buffering cell connected to another end of the signal wiring, adjacent to the second side of the function block.

13. A method for manufacturing a semiconductor integrated circuit

comprising:

arranging a plurality of function blocks on a substrate;

extracting a first function block with minimum signal loss in the function blocks in a signal wiring route;

extracting a second function block arranged near the first function block;

arranging a signal wiring which passes obliquely relative to a first side and a second side adjacent to the first side of the second function block;

determining whether a length of the signal wiring exceeds the signal wiring length limitation;

determining whether signal timing satisfies a design rule at least when the length of the signal wiring exceeds the signal wiring length limitation;

determining whether a buffering cell can be arranged when the signal timing fails to satisfy the design rule; and

arranging a first buffering cell connected to one end of the signal wiring, adjacent to the first side of the second function block and a second buffering cell connected to another end of the signal wiring, adjacent to the second side of the second function block.